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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,480	09/27/2001	Kaoru Awaka	TI-33253 (032350.B345)	8718

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,480	AWAKA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,9,10 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,9,10 and 18-20* is/are rejected.

7)☒ Claim(s) *3 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/10/2006.

2. Claims 1, 3, 9-10, 12, and 18-20 are pending in this application. Claims 1, 10, and 19-20 are independent claims. In Amendment, claims 2, 4-8, 11, and 13-17 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 9-10, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hansen et al. (U.S. 2003/01110197 A1).

Re claim 1, Hansen et al. disclose in Figure 2 a multiply-accumulate module (e.g. Figure 2 with 212 ACC as accumulator) comprising: a multiply-accumulate core (e.g. Figure 2), wherein multiply-accumulate core (e.g. Figure 2) comprises: a plurality of Booth encoder cells (e.g. Figure 3 and page 3 right column paragraph 0043); a plurality of Booth decoder (e.g. 201 Figure 2) cells connected to at least encoder cells (e.g. 303 in Figure 3), plurality of Booth decoder cells including at least one first Booth decoder cell

and at least one of Booth decoder cell, at least one first Booth decoder cell structurally the same as at least one second Booth decoder cells (e.g. page 3 right column paragraph 0042); a plurality of Wallace tree cells (e.g. paragraph 0059 and 202-211 in Figure 2) one of Booth decoder cells, connected to at least plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, at least one first Wallace tree cell structurally the same as at least one second Wallace tree cell (e.g. 204 and 207 in Figure 2); wherein multiply-accumulate module includes at least one critical path (e.g. any path in Figure 2 would be a critical path as reason under 112 rejection above), the at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal travel from an input of multiply-accumulate core to an output of multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from input of multiply-accumulate core signal to travel from input of multiply-accumulate core to output of multiply-accumulate core, wherein predetermined amount of time is less than a longest amount of time (e.g. translate into mathematical term $t_{pre} < t_{cri} < t_{lon}$ wherein t_{pre} is the predetermined time, t_{cri} is the critical time, and t_{lon} is the longest time; t_{cri} is the path to generate the first output, t_{lon} is the path to generate the last output, t_{pre} is any arbitrary number less than t_{cri}); wherein at least one first Wallace tree cell or at least one first Booth decoder cell are disposed on at least one critical path (e.g. the critical path running through 4-2 add in Figure 2); wherein at least one second Wallace tree cell and at least one second Booth decoder cell are not disposed on any of at least one critical path (e.g. the mux would route through at least one Wallace cell);

wherein at least one first Wallace tree or at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises second plurality of transistors (e.g. inherently these Wallace cells are structured with transistors as logic gates for forming an adder as an example), and a width of at least one of first plurality of transistors of at tleast one first Wallace tree cell or at least one first Booth decoder cell is greater than width of a corresponding one of second plurality transistors of a corresponding one of at least one second Wallace tree cell and at least one second Booth decoder cell (e.g. it is impossible to manufacture all transistors with exact same width).

Re claim 9, Hansen et al. further disclose in Figure 2 at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit (e.g. Figure 3).

Re claim 10, it is a parallel multiplier with limitations cited in claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 18, it is a parallel multiplier with limitations cited in claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 19, it is a method claim of claim 1. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 20, it is a method claim of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Allowable Subject Matter

5. Claims 3 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 01/10/2006 have been fully considered but they are not persuasive.

a. The applicant argues in page 9 for independent claims that the cited reference by Hansen et al. does not disclose critical paths as cited in the claimed invention.

The examiner respectfully submits that there are multiple critical paths within the structure of this MAC. At least one critical paths is longest which can be set as the longest amount of time and at least one critical paths is shortest which can be set as the predetermined time. Thus, any other critical paths in between the shortest and longest critical paths meet the claimed invention.

b. The applicant argues in pages 10-11 for independent claims that the cited reference by Hansen et al. fails to disclose the differing transistor widths dependent upon whether the cell is within a critical path. In addition, the predetermined time and the width of the first and second Wallace transistors are tied together as critical path.

The examiner respectfully submits that the language of independent claims do not define or disclose clearly the relationship between the predetermined time involving critical path and the differing width of transistors as argued by the applicant.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

February 3, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100